

Customer N : 31561
Application No.: 10/605,360
Docket No.: 11760-US-PA

IN THE CLAIMS

Claim 1. (Original) A method for fabricating a metal oxide semiconductor field effect transistor, comprising:

providing a substrate, said substrate having a gate structure;

forming a drain region and a source region in said substrate, beside two sides of said gate structure, respectively;

forming a metal silicide layer on the surface of said gate structure, said drain region, and said source region;

forming a patterned block on said metal silicide layer above said gate structure, and forming a first dielectric layer above said substrate except said gate structure, wherein said patterned block is formed above a center of said gate structure and said metal silicide layer above said gate structure beside two sides of said patterned block is exposed;

removing a portion of said metal silicide layer and a portion of said gate structure by using said patterned block as a mask; and

forming a drain extension region and a source extension region in said substrate, said drain extension region and said source extension region being on two sides of said remaining gate structure.

Claim 2. (Original) The method of claim 1, wherein said step of forming said patterned block and said first dielectric layer includes performing a high density plasma chemical vapor deposition.

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Claim 3. (Original) The method of claim 1, wherein said patterned block and said first dielectric layer are silicon oxide.

Claim 4. (Original) The method of claim 1, wherein said metal silicide layer exposed on the one side of said patterned block and on the other side of said patterned block are symmetrical and have a same area.

Claim 5. (Original) The method of claim 1, wherein said step of forming said patterned block and said first dielectric layer further comprises

forming a dielectric material layer; and

etching back said dielectric material layer.

Claim 6. (Original) The method of claim 1, wherein after said step of forming said drain extension region and said source extension region, the method further comprises forming a second dielectric layer on said substrate.

Claim 7. (Currently amended) The method of claim 1, wherein after said step of forming said drain ~~extension~~ region and said source ~~extension~~ region and before said step of forming said metal silicide layer, the method further comprises

forming a lining layer on said substrate to cover said gate structure, said drain region, and said source region; and

etching back said lining layer to have said lining layer being remained on a sidewall of said gate structure.

Claim 8. (Original) A method for reducing a line width of a gate, comprising:
providing a substrate, said substrate having a gate structure;

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forming a patterned block on said gate structure with a high density plasma chemical vapor deposition, said patterned block being formed on the center of said gate structure, wherein said gate structure beside two sides of said patterned block is exposed; and

removing a portion of said gate structure by using said patterned block as a mask.

Claim 9. (Original) The method of claim 8, wherein said patterned block is silicon oxide.

Claim 10. (Original) The method of claim 8, wherein said gate structure exposed on the one side of said patterned block and on the other side of said patterned block are symmetrical and have a same area.

Claim 11. (Original) The method of claim 8, said step of forming said patterned block further comprises;

forming a dielectric material layer with a high density plasma chemical vapor deposition ; and

etching back said dielectric material layer to form said patterned block.